

FIG.1

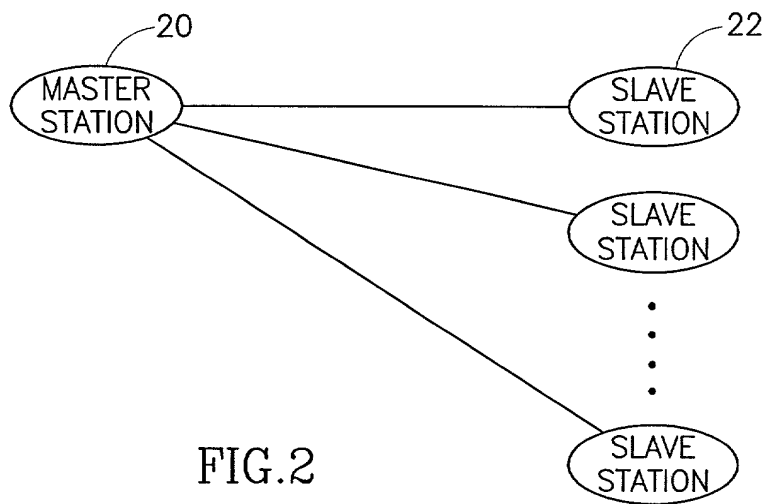
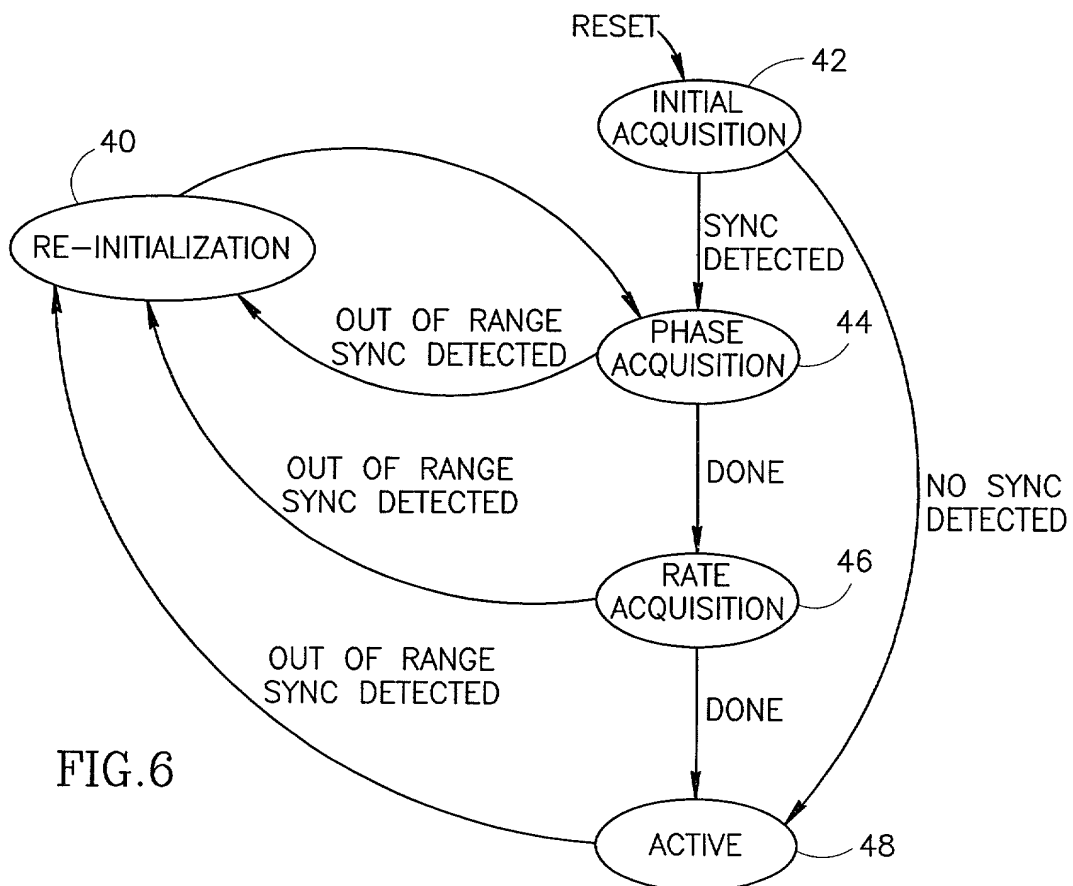
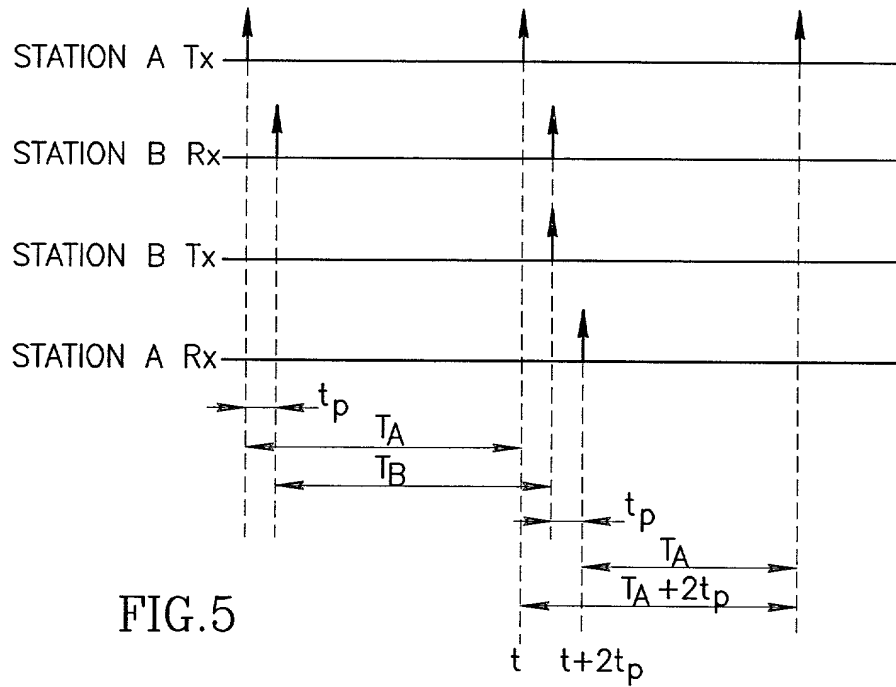


FIG.2

Timing diagram for a slave receiver. The diagram shows three horizontal lines representing the signals: MASTER Tx, SLAVE Rx, and SLAVE Tx. Vertical dashed lines mark key events: t_p (propagation delay), $t(n)$ (transmission time), and t_{RECEIVED} (reception time). Horizontal double-headed arrows indicate durations T_M (Master frame time) and T_S (Slave frame time).

The diagram shows two stations, Station A (labeled 30) and Station B (labeled 32), connected by two curved lines. The top line is labeled 'MASTER' near Station A and 'SLAVE' near Station B. The bottom line is labeled 'SLAVE' near Station A and 'MASTER' near Station B. This indicates a dual-master/slave configuration where each station can act as a master to the other.

FIG.4



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graph TD
    48([INITIAL ACQUISITION METHOD]) --> 50[SET INTERNAL CLOCK PERIOD T TO T_NOMINAL]
    50 --> 52[SELECT RANDOM WAIT TIME]
    52 --> 54{WAIT FOR RECEIPT OF ONE OR MORE SYNCHRONIZATION SIGNALS}
    54 -- RECEIVED --> 56[SET T_RECEIVED TO THE EARLIEST SYNCHRONIZATION SIGNAL RECEIVED]
    56 --> 58[SET INTERNAL CLOCK PHASE t TO t_RECEIVED + T]
    58 --> 60([PHASE ACQUISITION STATE])
    54 -- TIMEOUT --> 62[SET t TO AN ARBITRARY VALUE]
    62 --> 64[t = t + T]
    64 --> 66([ACTIVE STATE])

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FIG.8

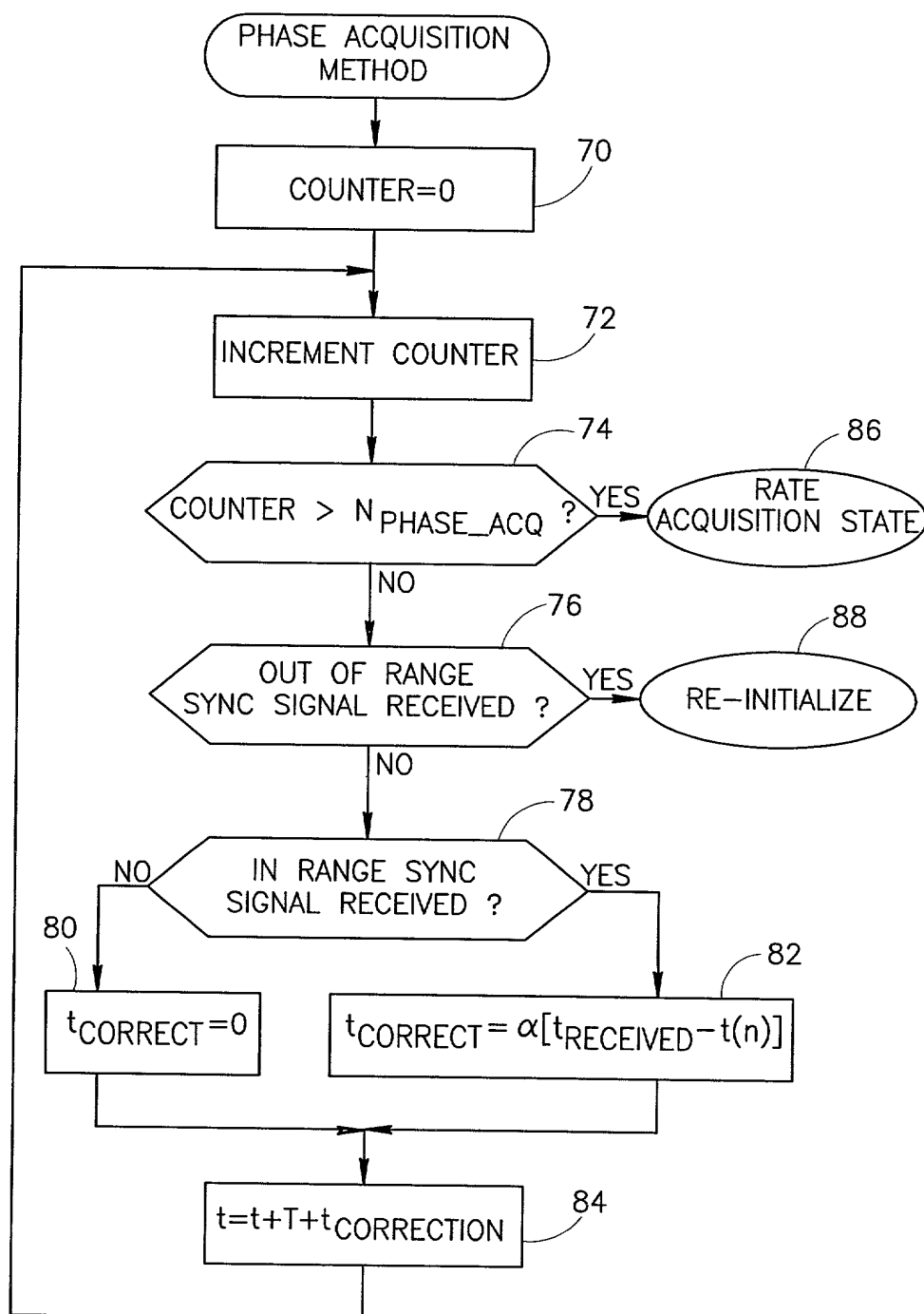


FIG.9

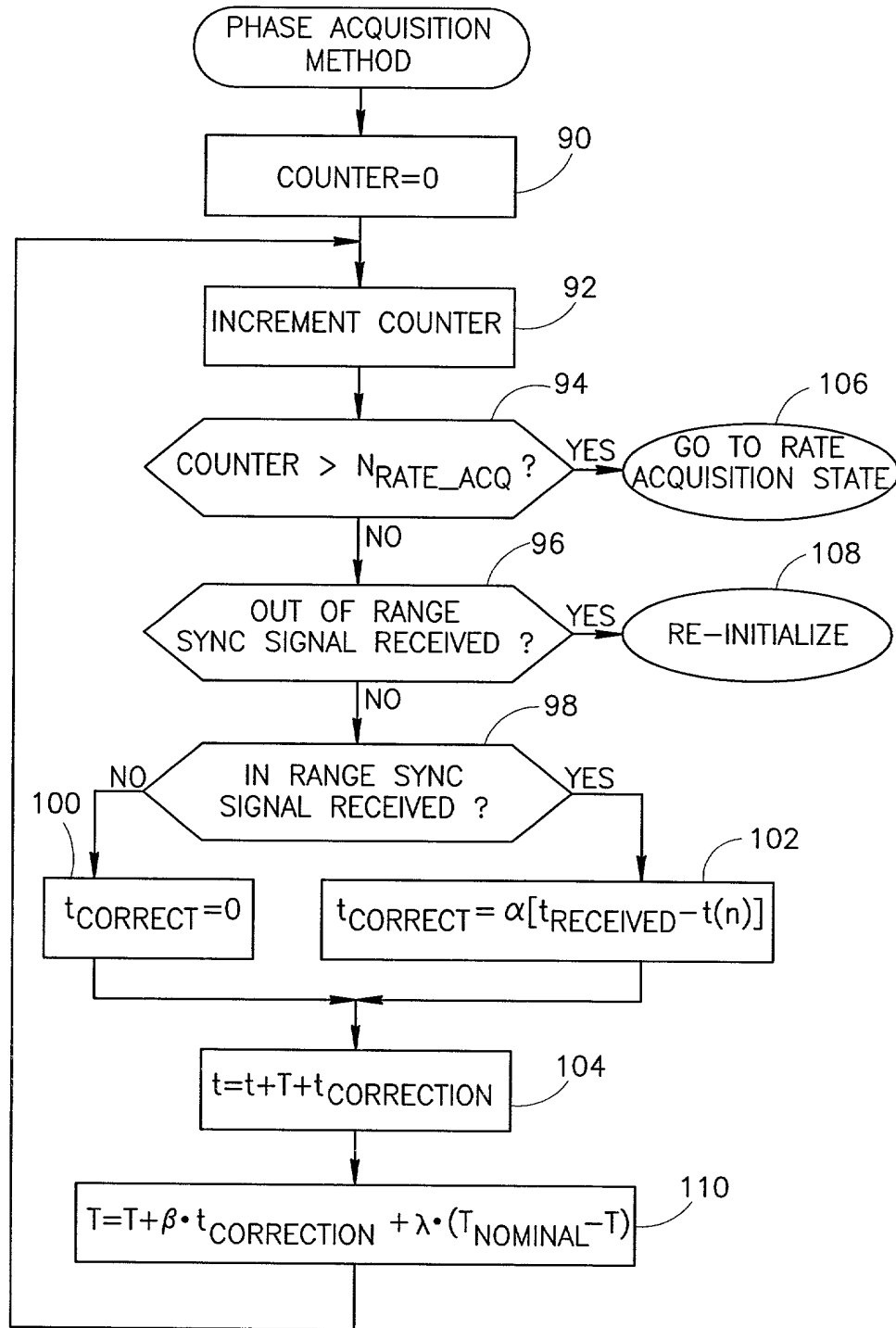


FIG.10

FIG. 11

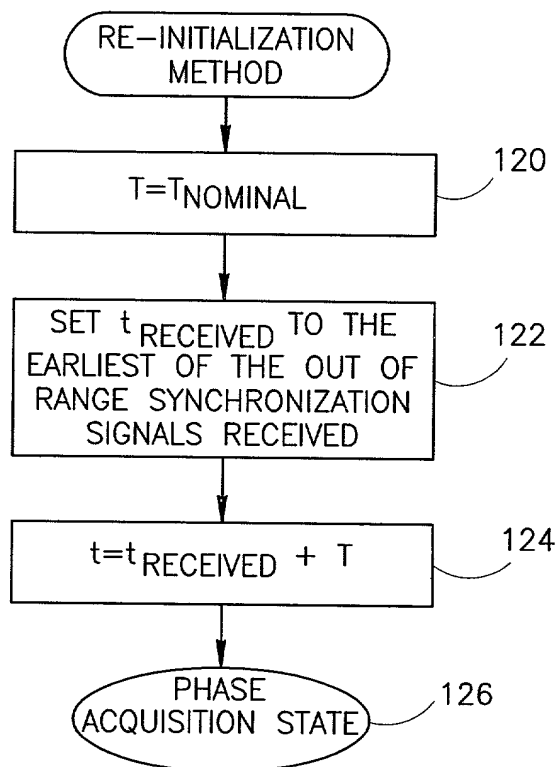


FIG.11

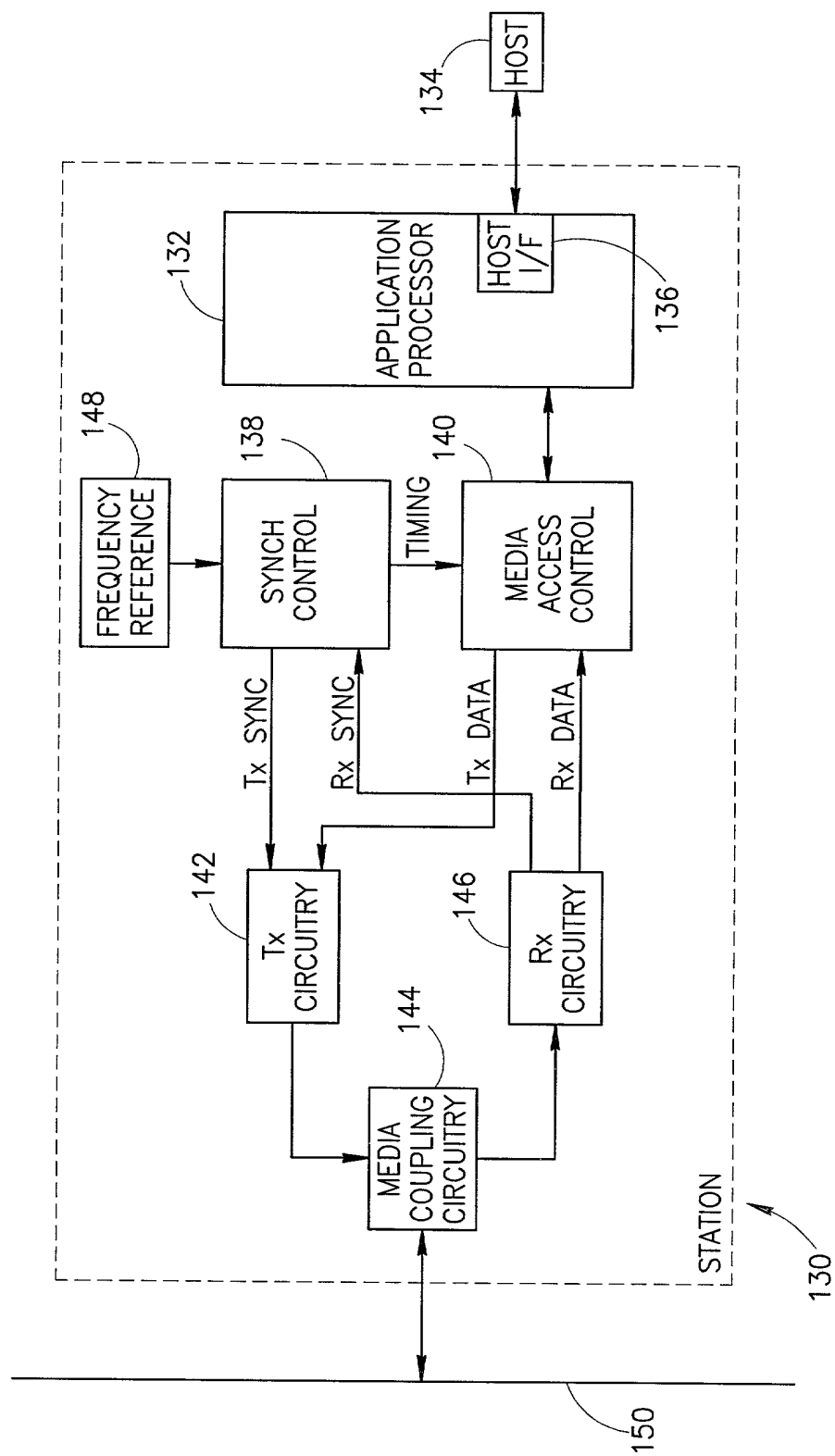


FIG.12